

Form PTO-1449 <b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b> <i>(Use several sheets if necessary)</i>			Docket Number (Optional) 4308.4US (99-1199.04/US)	Application Number 10/791400		
			Applicant John T. Moore			
			Filing Date March 2, 2004	Group Art Unit 2824		
<b>U.S. PATENT DOCUMENTS</b>						
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
CSW	5,567,638	10/1996	Lin et al.	438	592	
	5,633,177	05/1997	Anjum	438	301	
	6,013,553	01/2000	Wallace et al.	438	287	
	6,017,808	01/2000	Wang et al.	438	528	
	6,136,654	10/2000	Kraft et al.	438	287	
	6,140,024	10/2000	Misium et al.	430	314	
	6,251,761	06/2001	Rodder et al.	438	591	
	6,261,973	07/2001	Misium et al.	438	775	
	6,342,437	01/2002	Moore	438	474	
CDW	6,528,396	03/2003	Moore	438	484	
<b>FOREIGN PATENT DOCUMENTS</b>						
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation
						YES
<b>OTHER DOCUMENTS</b> <small>(Including Author, Title, Date, Pertinent Pages, Etc.)</small>						
CDW	Al-Shareef et al., "Device Performance of <i>in situ</i> Steam Generated Gate Dielectric Nitrided by Remote Plasma Nitridation", Applied Physics Letters, Volume 78, Number 24, June 11, 2001, pps. 3875-3877.					
	Al-Shareef et al., "Plasma Nitridation of Very Thin Gate Dielectrics", Microelectronic Engineering, 59, 2001, pps 317-322.					
CDW	Hattangady et al., "Ultrathin Nitrogen-Profile Engineered Gate Dielectric Films", IEDM Tech. Dig., 1996, pps. 495-498.					
EXAMINER	DATE CONSIDERED					
Christian W. Son	9/8/04					
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.						

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						YES
<b>OTHER DOCUMENTS</b> <small>(Including Author, Title, Date, Pertinent Pages, Etc.)</small>						
CDW	Koh et al., "Plasma-Engineered Si-SiO <sub>2</sub> Interfaces: Monolayer Nitrogen Atom Incorporation by Low-Temperature Remote Plasma-Assisted Oxidation in N <sub>2</sub> O", Surface and Coatings Technology, 1998; pps. 1524-1528.					
	Lucovsky et al., "Plasma Processed Ultra-Thin SiO <sub>2</sub> Interfaces for Advanced Silicon NMOS and PMOS Devices: Applications to Si-Oxide/Si Oxynitride, Si-Oxide/Si Nitride and Si-Oxide/Transition Metal Oxide Stacked Gate Dielectrics", Thin Solid Films, 2000, pps. 217-227.					
	Mehrotra et al., "A 1.2V, Sub-0.09μm Gate Length CMOS Technology", IEDM Tech. Dig., 1999, pps. 419-422.					
	Niimi et al., "Monolayer-Level Controlled Incorporation of Nitrogen in Ultrathin Gate Dielectrics Using Remote Plasma Processing: Formation of Stacked "N-O-N" Gate Dielectrics", J. Vac. Sci. Technology B 17, Nov/Dec 1999, pps. 2610-2621.					
CDW	Ting et al., "The Effect of Remote Plasma Nitridation on the Integrity of the Ultrathin Gate Dielectric Films in 0.13 μm CMOS Technology and Beyond", IEEE Electron Device Letters, Vol. 22, No. 7, July 2001, pps. 327-329.					
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Christian Wilson	9/8/04					
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